REMARKS/ARGUMENTS

Claims 163-164, 166-171, 173 and 176-210 are pending in the application, of which Claims 163, 179, and 197 are the independent claims. Claims 1-162, 165, 172, 174, and 175 were previously cancelled without prejudice. No claims have been added herein. Claims 163, 164, 171, 173, 176, 179-181, 184, 190-199, 201, 203, 205, 206 and 208 have been amended herein. No new matter is believed to be added by this paper. Entry hereof and early passage to issue are respectfully requested.

Claim Rejections – 35 USC §103

Claims 163-164, 168, 171, 173, 176 are rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Eichelberger (U.S. Patent 6,396,148) in view of Gupta (U.S. Patent 6,383,858); Claims 166-170 and 178 are rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Eichelberger with Gupta and further in view of Cole (U.S. Patent 5,745,984); Claim 177 is rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Eichelberger with Gupta and further in view of Wagner (U.S. Patent 5,196,377); Claims 179, 184, 187-194, 196-199, 201, 203, 205, 206, and 208-210 are rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Eichelberger with Gupta and further in view of Wachtler (U.S. Patent 6,707,124); Claims 180-183, 185, 186, 200, 202, and 204 are rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Eichelberger with Gupta and Wachtler and further in view of Cole; Claims 195 and 207 are rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Eichelberger with Gupta and Wachtler and further in view of Wagner. Reconsideration and withdrawal of these rejections are respectfully requested.

Amended claim 163 is drawn to a chip package comprising a die-surrounding layer and a die between a first portion of the die-surrounding layer and a second portion of the die-surrounding layer, wherein the die has a top surface substantially coplanar with a top surface of the die-surrounding layer, wherein said die comprises a metal pad at a top side of said die. The chip package also includes a first dielectric layer on the top surface of the die and the top surface of the die-surrounding layer, and a patterned metal layer over the first dielectric layer, the top surface of the die and the top surface of the die-surrounding layer. The patterned metal layer is

connected to the metal pad of the die through an opening in the first dielectric layer, wherein said patterned metal layer comprises a portion of a comb-shaped capacitor. The chip package also includes a second dielectric layer on the patterned metal layer and over the first dielectric layer, the top surface of the die and the top surface of the die-surrounding layer.

Amended claim 179 is drawn to a chip package comprising a die-surrounding layer and a die between a first portion of the die-surrounding layer and a second portion of the die-surrounding layer. The die has a top surface substantially coplanar with a top surface of the die-surrounding layer, wherein said die comprises a first metal pad at a top side of said die and a second metal pad at said top side. The chip package also includes a first dielectric layer on the top surface of the die and on the top surface of the die-surrounding layer, and a patterned metal layer over the first dielectric layer, the top surface of the die and the top surface of the die-surrounding layer, wherein the patterned metal layer is connected to the first metal pad of the die through a first opening in the first dielectric layer. The patterned metal layer is connected to the second metal pad of the die through a second opening in the first dielectric layer. The first metal pad is connected to the second metal pad through the patterned metal layer, wherein the patterned metal layer comprises a portion of a passive device.

Amended claim 197 is drawn to a chip package comprising a die-surrounding layer and a die between a first portion of the die-surrounding layer and a second portion of the die-surrounding layer. The die has a top surface substantially coplanar with a top surface of the die-surrounding layer, wherein said die comprises a first metal pad at a top side of said die and a second metal pad at said top side. The chip package also includes a first dielectric layer on the top surface of the die and on the top surface of the die-surrounding layer, and a patterned metal layer over the first dielectric layer, the top surface of the die and the top surface of the die-surrounding layer. The patterned metal layer comprises a ground piece connected to the first metal pad of the die through a first opening in the first dielectric layer, and connected to the second metal pad of the die through a second opening in the first dielectric layer. The first metal pad is connected to the second metal pad through the ground piece, wherein the patterned metal layer comprises a portion of a passive device.

The applied references, either alone or in combination, are not seen to disclose or suggest the foregoing features of each of amended independent Claims 163, 179 and 197.

In this regard, the Office Action includes the statement that "There is also clear motivation for practicing multiple ICs as Gupta in a packaging scheme as Eichelberger for enabling electroless plating of final bond pads." Office Action, p. 5, line 21 through p.6, line 1.

Applicants respectfully disagree with this statement because Eichelberger's electroless plating that is performed in a package-level process, performed after dies have been cut from a wafer, would not be enabled to form ICs performed in a wafer-level process, like Gupta's process, having been performed before a wafer is cut into dies, because the metal trace made by a package-level process is limited to be formed in a dramatically larger scale than the metal trace made by a wafer-level process is formed. The mechanical and electrical properties of the metal trace made in a wafer-level process are significantly different from those of the metal trace made in a package-level process, which would cause a circuitry adapted to be formed in a wafer-level process because the performance of the circuitry formed in a wafer-level process cannot be attained by the same formed in a package-level process, and alternatively which would cause the other circuitry adapted to be formed in a package-level process because the performance of the other circuitry formed in a package-level process cannot be attained by the same formed in a wafer-level process. Accordingly, the circuitry made by a wafer-level process, like Gupta's process, would not be considered to be formed for a package-level circuitry, like the one made by Eichelberger's metallization 108.

The Office Action also includes the statement that "It would not have been unobvious to practice multilevel metalization[sic] over a die of Eichelberger from Gupta. In fact Gupta shows how to enable multilevel metallization with comb capacitor structure over dies. Together the references suggest integrated circuits with comb-shaped capacitors and isolation material around integrated circuits in a package as Eichelberger with Gupta." Office Action, p. 6, lines 7-11.

Applicants respectfully disagree with this statement. As mentioned above, Gupta's multilevel metallization made in a wafer-level process would not be considered to be performed over Eichelberger's dies 102 in a package-level process. Instead, only if, *in arguendo*, the

multilevel metallization is made in a package-level process, would the multilevel metallization be motivated to be applied into Eichelberger's package-level process.

The Office Action further includes the statement that "the claims are drawn to structure rather than a process. Regardless of the process of manufacture, packages with multiple dies including comb-shaped capacitors are obvious from the suggestions of the references, as integrated capacitors are essential for small IC circuitry requiring large capacitances, such as the circuit of Gupta." Office Action, p.5, lines 9-12.

Applicants respectfully disagree with this statement. Circuitry performed in a wafer-level process would not be considered to be readily performed in a package-level process. Circuitry performed in a wafer-level process is closer to transistors provided in a wafer, but circuitry performed in a package-level process is farther away from transistors provided in a die, which would cause some circuitries adapted to be performed in a wafer-level process but not to be adapted to be performed in a package-level process, as mentioned above. The metal trace made by a package-level process is limited to be formed in a dramatically larger scale than the metal trace made by a wafer-level process is formed, so the mechanical and electrical properties of the metal trace made in a wafer-level process are significantly different from those of the metal trace made in a package-level process, which would also cause some circuitries adapted to be performed in a wafer-level process but not to be adapted to be performed in a package-level process, as mentioned above. Based on the above concerns, comb-shaped capacitors formed in a wafer-level process, like Gupta's comb-shaped capacitors, would not be considered to be formed in a package-level process, like Eichelberger's process.

In reply to page 14 of the Applicants argument that Gupta does not teach a capacitor over the die, the Office Action includes the statement that "This is not persuasive as Gupta discloses capacitor 100 over silicon die material 418. The comb capacitor is also part of the metallization over the die. Taken together, the references suggest capacitors in metallization over dies in a planarized multichip package." Office Action, p.6, lines 12-16.

Applicants respectfully disagree with this statement because Gupta does not teach the step of forming a capacitor over a die, but instead teaches the step of forming a capacitor over a

semiconductor wafer substrate 418. See Gupta, Fig. 4 and col. 4, lines 49 and 50. Gupta's semiconductor wafer substrate 418 is used to have Gupta's interconnects and dielectric layers formed thereover in a wafer-level process. After a cutting process, Gupta's semiconductor wafer substrate 418 would be separated into multiple units for a subsequent package-level process and therefore would not be deemed to be analogous to a die, such as Eichelberger's integrated circuit chip 102, typically cut from a wafer and used for a subsequent package-level process, like Eichelberger's process.

In view of the above, amended independent Claims 163, 179 and 197 are believed to be allowable over the applied references. Reconsideration and withdrawal of the rejections of Claims 163, 179 and 197 are therefore respectfully requested.

The other claims currently under consideration in the application are dependent from the independent claims discussed above and therefore are believed to be allowable over the applied references for at least similar reasons. Because each dependent claim is deemed to define an additional aspect of the invention, the individual consideration of each on its own merits is respectfully requested.

The absence of a reply to a specific rejection, issue, or comment does not signify agreement with or concession of that rejection, issue, or comment. In addition, because the arguments made above may not be exhaustive, there may be other reasons for patentability of any or all claims that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment or cancellation of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment or cancellation.

CONCLUSION

In view of the Amendments and Remarks herein, Applicants submit that the application is in condition for allowance and respectfully request a notice to this effect. Should the Examiner have any questions, please call the undersigned at the phone number listed below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 502624 and please credit any excess fees to such deposit account.

Respectfully submitted,
McDERMOTT WILL & EMERY LLP

/Dennis A. Duchene/
Dennis A. Duchene
Registration No. 40,595

18191 Von Karman Avenue, Suite 500
Irvine, CA 92612-7108
Phone: 949.851.0633
Facsimile: 949.851.9348
Date: June 27, 2011

Please recognize our Customer No. 89518 as our correspondence address.